Amendments to the Specification:

Please replace the paragraph beginning at page 1, line 11, with the following redlined paragraph:

In a modulator for digital mobile telecommunication, the pulse shaping interpolation filtering is required in order to prohibit an inter-symbol interference at the rear end of the modulator. Specially, in case of an IMT-2000 synchronous terminal modulator as a next-generation mobile communication system, as a 1-bit output of four channels is ~~multiplexed~~ multiplied by a gain within a single chip, channels are added two by two and the results are experienced by OCQPSK modulation, two FIR filters having n-bit input are required.

Please replace the paragraph beginning at page 1, line 24, with the following redlined paragraph:

Explaining in more detail, 1-bit input of four channels CH1, CH2, CH3 and CH4 is Walsh-covered by Walsh quadrature codes Walsh2, Walsh3 and Walsh4 10 by means of exclusive-OR gates 11, 12 and 13 for channel discrimination. Next, the 1-bit input is inputted to the gain stage 20 in which the gains G1, G2, G3 and G4 of respective channels are multiplied by means of the multipliers 21, 22, 23 and 24, in order to adjust gains of respective channels for channel discrimination. Then, the outputs of n-bits type from the gain stage are added two by two in the adders 31 and 32 in the channel adder 30, thereby producing two quadrature signals DI and DQ.

Please replace the paragraph beginning at page 2, line 5, with the following redlined paragraph:

These two quadrature DI and DQ signals are modulated in the OCQPSK modulator 40. The OCQPSK modulator 40 includes a PN spreader 41 using PN sequence generated in a long & short PN generator 49, ~~and~~ a complex adder 42 for performing a complex multiplication for the PN sequence based on an OCQPSK modulation scheme, multipliers 43, 44, 45 and 46, and adders 47 and 48. The outputs from the OCQPSK modulator 40 are inputted, in a n-bit type, to FIR filter 50. The FIR filter 50 is consisted of two FIR filters 51 and 52 each

having n-bits inputs for pulse shaping, where the outputs of n-bits type are FIR-filtered. The output signals from the two FIR filters 51 and 52 are then inputted to D/A converters 60 and 61 of an analog chip, modulated 62 and 63, multiplied by gain 64, and outputted.

Please replace the paragraph beginning at page 5, line 1, with the following redlined paragraph:

In order to accomplish the objects, a 108-tap 1:4 interpolation FIR filter device for digital mobile communication according to the present invention is characterized in that it comprises four shift registers for ~~shifting/storing~~ shifting and storing 1-bit filter inputs each inputted from four channels to produce 27-bit parallel data, respectively; a selector for sequentially selecting the outputted parallel data of the four channels one by one; an address generator for receiving the 27-bit parallel data outputted from the selector to produce addresses depending on look-up tables of each of coefficient groups; four look-up table groups for generating filter outputs of the coefficient groups using the addresses generated in the address generator; a pipeline ~~registers~~ register I for delaying filter outputs per coefficient groups outputted from the four look-up table groups; a group selector for serially transforming the delayed outputs from the pipeline ~~registers~~ register I, channel by channel; and a pipeline ~~registersII~~ register II for delaying the output from the group selector to match the time of the filter output per channel.

Please replace the paragraph beginning at page 6, line 10, with the following redlined paragraph:

Referring now to Figure 3, there is showing that a construction of a 108-tap 1:4 interpolation FIR filter of a single bit input for four channels according to one embodiment of the present invention. The 108-tap 1:4 interpolation FIR filter includes an input shift register & selector 100, an address generator 200, a look-up table ~~group0~~ group 0 300, a look-up table ~~group3~~ group 3 400, a look-up table ~~group1~~ group 1 500 and a look-up table ~~group2~~ group 2 600, for producing filter coefficients group by group using a look-up table and operating them, a

pipeline ~~registersI~~ register I 700, a group selector 800~~)~~, and a pipeline ~~registersII~~ register II 900.

Please replace the paragraph beginning at page 9, line 19, with the following redlined paragraph:

The look-up table ~~group0~~ group 0 300 is a block for creating the filtering result of the filter coefficient ~~group0~~ group 0 filter by means of the look-up table and an operation, and its operation is as follows.

Please replace the paragraph beginning at page 10, line 7, with the following redlined paragraph:

Meanwhile, the look-up table ~~group3~~ group 3 400 performs the following operations in order to calculate LUT0_2 and LUT0_3 that are removed by the coefficient symmetry characteristic by operating the filtering result of the filter coefficient ~~group3~~ group 3 and the look-up table.

Please replace the paragraph beginning at page 10, line 18, with the following redlined paragraph:

The calculating result L3 of the ALU2 404 and the calculating result of the ALU2 304 are inputted to the ADD 305, which then produces LO. The L0 and 0C outputted from the LUT0_C 303 are inputted to the ALU1 306, and the LO and the 3C outputted from the LUT3_C 403 are inputted to the ALU1 405. The output value of the ALU1 405 is determined by B[2]. If B[2] = 0, the output of the ALU1 306 is L0 + 0C and the output of the ALU1 405 is L0 + 3C. On the other hand, if B[2] = 1, the output of the ALU1 306 is L0 - 0C ~~OC~~ and the output of the ALU1 405 is L0 - 3C. The REG 307, a register for storing G0, an output of the look-up table ~~group0~~ group 0 by means of a rising edge of ck4, is used to buffer the output value of the look-up table ~~group0~~ group 0 300 twice accessed due to the symmetry of the coefficient. The ALU1 405 outputs G3, an output of the look-up table ~~group3~~ group 3.

Please replace the paragraph beginning at page 11, line 1, with the following redlined paragraph:

With the same method to the operation of the look-up table ~~group0~~ group 0 300 and the look-up table ~~group3~~ group 3 400, the look-up table ~~group1~~ group 1 500 and the look-up table ~~group2~~ group 2 600 are operated to produce filter outputs G0, G1, G2 and G3.

Please replace the paragraph beginning at page 11, line 6, with the following redlined paragraph:

The pipeline ~~registersI~~ register I 700 functions to delay filter outputs G0, G1, G2 and G3 for four look-up table groups generated parallel simultaneously depending on corresponding coefficient groups so as to sequentially output the filter outputs. The pipeline ~~registersI~~ register I 700 consist of ten registers REGs for storing input data at a negative edge of ck4. GO is delayed with four clocks via the four REGs and is outputted as R0, Gl is delayed with three clocks via the three REGs and is outputted as R1, G2 is delayed with two clocks via the two REGs and is outputted as R2, G3 is delayed one clock via one REG and is outputted as R3.

Please replace the paragraph beginning at page 11, line 23, with the following redlined paragraph:

The pipeline ~~registers II~~ register II 900 consists of ten registers REGs for storing at a negative edge of ck4. The pipeline register II 900 is used to in parallel match signals M0 ~ M3 of time delay, which are outputted from the group selector 800, by respective filter outputs. The final filter output FO0 of the channel 0 produces M0 with four clocks delayed, the final filter output FO1 of the channel 1 produces Ml with three clock delayed, the final filter output FO2 of the channel 2 produces M2 with two clocks delayed, and the final filter output FO3 of the channel 3 produces M3 with one clock delayed.